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1 Verification (co-organized with LA-TTTC): Exception handling in microprocessors using assertion libraries
Fernando Cortez Sica, Claudionor N. Coelho, José Augusto M. Nacif, Harry Foster, Antônio Otávio Fernandes
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**
Full text available: pdf(237.87 KB) Additional Information: full citation, abstract, references, index terms

In complex System-on-a-Chip (*SoC*) designs, designers often need to add new features into an original processor core, such as to extend the exception handling mechanism to consider exceptions in the remaining portion of the *SoC* design. We present in this paper a scalable architecture that can be used to add complex exception handling mechanisms in processor cores and how it can be used to extend the fixed set of exceptions found in microprocessor cores. This mechanism is based on th ...

Keywords: assertions, exceptions handling

2 Partial reconfigurable architectures: PaDReH: a framework for the design and implementation of dynamically and partially reconfigurable systems
Ewerson Carvalho, Ney Calazans, Eduardo Brião, Fernando Moraes
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**
Full text available: pdf(244.61 KB) Additional Information: full citation, abstract, references, index terms

Dynamically and Partially Reconfigurable Systems (DRSs) are those where any portion of the hardware behavior can be altered at application execution time. These systems have the potential to provide hardware with flexibility similar to that of software, while leading to better performance and smaller system size. However, the widespread acceptance of DRSs depends on adequate support to design and implement them. This work proposes a framework for DRS design and implementation named PADReH. The a ...

Keywords: dynamically and partially reconfigurable systems, partial bitstream generation, reconfiguration control, run-time reconfiguration

3 Low Cost Analog Testing of RF Signal Paths
Marcelo Negreiros, Luigi Carro, Altamiro A. Susin

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Full text available: pdf(374.70 KB) Additional Information: full citation, abstract, citings, index terms

A low cost method for testing analog RF signal paths suitable for BIST implementation in a SoC environment is described. The method is based on the use of a simple and low-cost one-bit digitizer that enables the reuse of processor and memory resources available in the SoC, while incurring little analog area overhead. The proposed method also allows a constant load to be observed by the circuit, since no switches or muxes are needed for digitizing specific test points. Mathematical background and ...

4 Retiming for Wire Pipelining in System-On-Chip

Chuan Lin, Hai Zhou

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(203.57 KB) Additional Information: full citation, abstract, index terms

At the integration scale of System-On-Chips (SOCs), the conflicts between communication and computation will become prominent even on a chip. A big fraction of system time willshift from computation to communication. In synchronoussystems, a large amount of communication time is spent onmultiple-clock period wires. In this paper, we explore retimingto pipeline long interconnect wires in SOC designs. Behaviorally,it means that both computation and communicationare rescheduled for parallelism. The ...

5 Modeling issues in the design of embedded systems: Architecture-level performance evaluation of component-based embedded systems

Jeffry T. Russell, Margarida F. Jacome

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(215.86 KB) Additional Information: full citation, abstract, references, index terms

A static performance evaluation technique is proposed to support early, architecture-level design space exploration for component-based embedded systems. The novel contribution is the use of a designer-specified evaluation scenario to identify a characteristic subset of system functionality that serves as a context for a rapid performance evaluation between candidate architectures. Fidelity is demonstrated with a case study that compares performance estimates of several candidate architectures t ...

Keywords: architecture-level, component-based, design space exploration, embedded system, performance evaluation, scenario

6 Energy-aware system design: A survey of techniques for energy efficient on-chip communication

Vijay Raghunathan, Mani B. Srivastava, Rajesh K. Gupta

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(94.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Interconnects have been shown to be a dominant source of energy consumption in modern day System-on-Chip (SoC) designs. With a large (and growing) number of electronic systems being designed with battery considerations in mind, minimizing the energy consumed in on-chip interconnects becomes crucial. Further, the use of nanometer technologies is making it increasingly important to consider reliability issues during the design of SoC communication architectures. Continued supply voltage scaling ha ...

Keywords: communication architectures, energy efficient design, low power design, power management, system-on-chip design

7 A Partition-Based Approach for Identifying Failing Scan Cells in Scan-BIST with Applications to System-on-Chip Fault Diagnosis

Chunsheng Liu, Krishnendu Chakrabarty

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Full text available: pdf(209.77 KB) Publisher Site

Additional Information: full citation, abstract, index terms

We present a new partition-based fault diagnosis technique for identifying failing scan cells in a scan-BIST environment. This approach relies on a two-step scan chain partitioning scheme. In the first step, an interval-based partitioning scheme is used to generate a small number of partitions, where each element of a partition consists of a set of scan cells. In the second step, additional partitions are created using an earlier-proposed random-selection partitioning method. Two-step partitioni ...

8 SystemC Modeling of a Bluetooth Transceiver: Dynamic Management of Packet Type in a Noisy Channel

Marco Caldari, Massimo Conti, Paolo Crippa, Giuliano Marozzi, Fabio Di Gennaro, Simone Orcioni, Claudio Turchetti

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2 DATE '03**

Full text available: pdf(249.47 KB) Publisher Site

Additional Information: full citation, abstract, index terms

High level design methodologies are needed to overcome the complexity of System on Chip design. In this paper the SystemC environment has been used to design a Bluetooth transceiver. The high simulation speed allowed a high level performance analysis of the IP developed and the definition of an algorithm for selecting the best packet type in presence of channel noise.

9 The A to Z of SoCs

Reinaldo A. Bergamaschi, John Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(209.48 KB)

Additional Information: full citation, abstract, references, citings, index terms

The exploding complexity of new chips and the ever decreasing time-to-market window are forcing fundamental changes in the way systems are designed. The advent of Systems-on-Chip (SoC) based on pre-designed intellectual-property (IP) cores has become an absolute necessity for embedded systems companies to remain competitive. Designing an SoC, however, is extremely complex, as it encompasses a range of difficult problems in hardware and software design. This paper explains a wide range of SoC iss ...

10 Rapid design space exploration of heterogeneous embedded systems using symbolic search and multi-granular simulation

S. Mohanty, V. K. Prasanna, S. Neema, J. Davis

June 2002 **ACM SIGPLAN Notices , Proceedings of the joint conference on Languages, compilers and tools for embedded systems: software and compilers for embedded systems**, Volume 37 Issue 7

Full text available: pdf(356.42 KB)

Additional Information: full citation, abstract, references, citings, index terms

In addition to integrating different Intellectual Property cores, heterogeneous embedded

systems provide several architecture knobs such as voltage, operating frequency, configuration, etc. that can be varied to optimize performance. Such flexibilities results in a large design space making system optimization a very challenging task. Moreover, such systems operate in mobile and other power constrained environments. Therefore, in addition to rapid exploration of a large design space a designer h ...

Keywords: binary decision diagram, design space, model integrated computing, modeling, multi-granular simulation, performance estimation, symbolic search

11 Cellular and Cryptographic Applications: Cryptographic rights management of FPGA intellectual property cores

Tom Kean

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: pdf(171.79 KB) Additional Information: full citation, abstract, references, index terms

As the capacity of FPGA's increases to millions of equivalent gates the use of Intellectual Property (IP) cores becomes increasingly important to control design complexity. FPGA's are becoming platforms for integrating a system solution from components supplied by independent vendors in the same way as printed circuit boards provided a platform for earlier generations of designers. However, the current commercial model for IP cores involves large up-front license fees reminiscent of ASIC NRE cha ...

Keywords: FPGA, cryptography, intellectual property, rights management

12 PACT 2001 workshops: Propagating constants past software to hardware peripherals in fixed-application embedded systems

Frank Vahid, Rilesh Patel, Greg Stitt

December 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 5

Full text available: pdf(483.89 KB) Additional Information: full citation, abstract, references, index terms

Many embedded systems include a microprocessor that executes a single program for the lifetime of the system. These programs often contain constants used to initialize control registers in peripheral hardware components. Now that peripherals are often purchased in intellectual property (core) form and synthesized along with the microprocessor onto a single chip, new optimization opportunities exist. We introduce one such optimization, which involves propagating the initialization constants past ...

Keywords: constant propagation, cores, embedded systems, intellectual property, low power, platforms, synthesis, system-on-a-chip, tuning

13 Detailed routing architectures for embedded programmable logic IP cores

Peter Hallschmid, Steven J. E. Wilton

February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Full text available: pdf(203.44 KB) Additional Information: full citation, abstract, references, citings, index terms

As the complexity of integrated circuits increases, the ability to make post-fabrication changes to fixed ASIC chips will become more and more attractive. This ability can be realized using programmable logic cores. These cores are blocks of programmable logic that can be embedded into a fixed-function ASIC or a custom chip. Such cores differ from stand-alone FPGAs in that they can take on a variety of shapes and sizes. With this in mind, we investigate the detailed routing characteris ...

Keywords: FPGA, SoC design, detailed routing, embedded cores, programmable logic

14 Trace-driven system-level power evaluation of system-on-a-chip peripheral cores

Tony D. Givargis, Frank Vahid, Jörg Henkel

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings, index terms

Our earlier work for fast evaluation of power consumption of general cores in a system-on-a-chip described techniques that involved isolating high-level instructions of a core, measuring gate-level power consumption per instruction, and then annotating a system-level simulation model with the obtained data. In this work, we describe a method for speeding up the evaluation further, through the use of instruction traces and trace simulators for every core, not just microprocessor cores. Our m ...

Keywords: cores, intellectual property, low power system design, parameterized architectures, system-level modeling, system-on-a-chip

15 A method to derive application-specific embedded processing cores

Olivier Hébert, Ivan C. Kraljic, Yvon Savaria

May 2000 **Proceedings of the eighth international workshop on Hardware/software codesign**

Full text available: pdf(101.67 KB) Additional Information: full citation, abstract, references, citings, index terms

The concept of system-on-a-chip is becoming increasingly popular for the integration of complex systems. New types of processor cores are now available that enable the designer to customize their processors for the target applications. These soft cores are not tightly coupled with the target application, and this leads to processing cores sub-optimal for their specific applications. This paper proposes a method to derive application-specific embedded processors from soft processor cores. Th ...

Keywords: configurable processor, custom core, embedded core, soft core, system-on-a-chip

16 MOCSYN: multiobjective core-based single-chip system synthesis

Robert P. Dick, Niraj K. Jha

January 1999 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(150.25 KB) Additional Information: full citation, citings, index terms

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